Design and Fabrication of SiO_2/Si_3N_4 Integrated-Optics Waveguides on Silicon Substrates

Douglas Anderson Pereira Bulla, Ben-Hur Viana Borges, Murilo Araujo Romero, Nilton Itiro Morimoto, and Luiz Gonçalves Neto

***Abstract*—In this paper, the design and fabrication of silicon-based optical waveguides are revisited. The goal is to develop a novel design and deposition process to minimize leakage losses. Interface roughness and Si_3N_4 stoichiometry are examined. The optical loss is measured and contributions from scattering and absorption are determined.**

***Index Terms*—Integrated optics, silicon, waveguides.**

I. Introduction

Silicon opto-electronics have attracted a great deal of interest in recent years [1]. The motivation for fabricating optical devices on silicon substrates is mainly due to the mature silicon processing technology, with availability of low-cost high-purity wafers and, mostly important, the possibility of integrating these optical devices with microelectronic and/or micromechanical elements. Compared to purely electronic solutions, silicon opto-electronics technology offers several advantages, including robustness to hazardous environments, immunity to electromagnetic interference, compactness, and light weight.

Silicon-based optical devices have been fabricated on different material systems [2]–[4]. However, in each case, the optical waveguide structures present a lower refractive index cladding layer, usually SiO_2, on top of the higher index silicon substrate. Thus, care must be taken in order to control the power leakage to the substrate, which can cause a severe optical power penalty on the propagating mode.

Usually, this leakage control is performed by making the lower SiO_2 cladding thick enough to act as an optical buffer. Nevertheless, thick silicon oxide films are difficult to obtain because high stress will promote film cracking and pilling [5].

In the following sections, we will present the fabrication process for our $SiO_2/Si_3N_4/SiO_2$ optical waveguides. Leakage losses are kept under control by the use of a careful design procedure, as well as by the development of a novel plasma-enhanced chemical vapor deposition (PECVD) technique [6], which allows, if necessary, the deposition of an SiO_2 buffer layer with thickness well above 1 μm. Characterization results are presented and interface roughness and Si_3N_4 stoichiometry are examined. The optical loss is measured and contributions from scattering and absorption are determined.

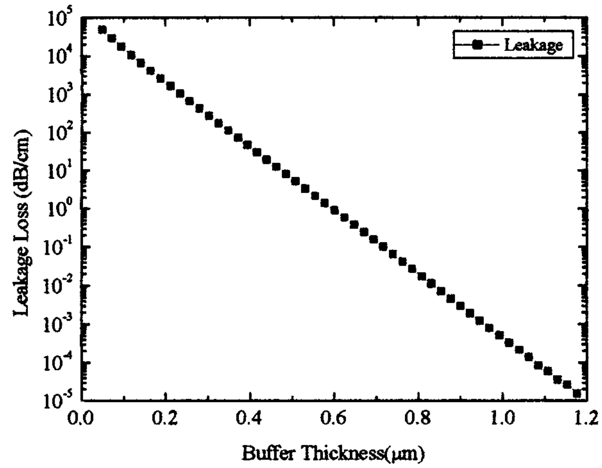

Fig. 1. Leakage loss as a function of the SiO_2 buffer thickness.

II. Structure Design

A. Leakage Evaluation

When a low index waveguide is fabricated on top of a higher index substrate, it will face a leakage loss problem. Therefore, if low-loss waveguides are desired, it is of paramount importance to reduce this leakage effect. The different ways of reducing optical power leakage are: 1) to increase the buffer layer thickness, i.e., increase the thickness of the layer separating the waveguide core layer from the substrate and 2) to increase the refractive index difference between guiding and cladding layers.

The approach taken in this paper consists of selecting silicon nitride as the waveguide core layer in order to take advantage of the relatively high refractive index contrast between Si_3N_4 and SiO_2. Next, a transfer matrix formalism, described in more detail in [7], is used to compute the SiO_2 optical buffer layer thickness required to reduce the leakage loss to a negligible level in the designed structure. The simulated results are shown in Fig. 1. As can be seen, for this particular material system, a

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D. A. P. Bulla and N. I. Morimoto are with the Laboratório de Sistemas Integráveis, Escola Politécnica, University of São Paulo, 05508-900 São Paulo SP, Brazil (e-mail: bulla@lsi.usp.br).

B.-H. V. Borges, M. A. Romero, and L. Gonçalves Neto are with the Departamento de Engenharia Elétrica, Escola de Engenharia de São Carlos, University of São Paulo, 13560-250 São Carlos SP, Brazil (e-mail:Muriloa@sel.eesc.sc.usp.br).

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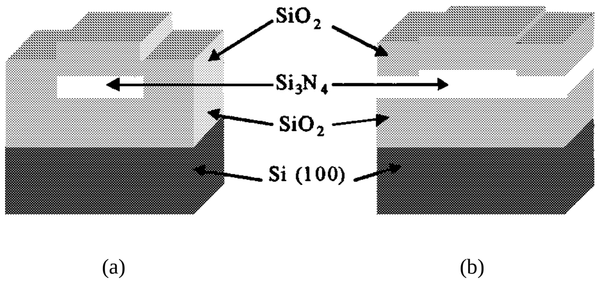

Fig. 2. Schematic waveguide structures. Single or multimode characteristics resulted from the distinct lateral field confinement characteristics.

buffer layer thickness of only 1.0 μm can effectively eliminate the leakage loss problem.

B. Fabricated Waveguides

The fabricated waveguide structures are shown schematically in Fig. 2. The layer sequence starts with the dry thermal deposition of 1-μm-thick silicon–oxide buffer layer on top of a 3-in-diameter p-type $\langle 100 \rangle$; 5–15-$\Omega \cdot$cm silicon substrate, which was cleaned using a standard rapid thermal annealing (RTA) treatment and subsequently washed in an HF solution to remove the native oxide. Over the buffer layer, a stoichiometric 0.14-μm-thick silicon–nitride thin film is deposited by the use of low-pressure chemical vapor deposition (LPCVD). Next, the channel and rib waveguides are defined by reactive ion etching (RIE) and buffered oxide etchant (BOE) respectively. Finally, a 0.2-μm tetraethylorthosilicate plasma-enhanced chemical vapor deposition (TEOS PECVD) SiO_2 layer [6] is deposited as upper cladding of the optical devices.

It is worth mentioning that this PECVD process, when combined with a RTA treatment, has already allowed us to successfully obtain silicon–oxide layers up to 4-μm thick [6]. The choice of silicon nitride as the guiding layer of the structures described in this paper made it possible to keep the thickness of the buffer SiO_2 layer around 1 μm without significant power leakage and, as a consequence, to use a simpler dry thermal growth process for the deposition of the lower waveguide cladding. However, in several instances where the refractive index contrast between the core and cladding is not so high, a PECVD process like ours will be extremely useful for buffer layer deposition.

III. Experimental Characterization

In order to assess film quality, the SiO_2/Si_3N_4 interface roughness was measured by a grazing incidence X-ray reflectometry (GIXR) technique [8]. Fig. 3 shows the fitting of the GIXR data, yielding an rms roughness value of 0.35 nm. Next, the stoichiometry of the silicon–nitride core was determined by fitting the Rutherford backscattering spectrometry (RBS) spectrum with the RUMP simulator [9], yielding, as indicated in Fig. 4, the stoichiometric N/Si ratio of 4/3. Finally, Fig. 5 shows the scanning electron microscopy (SEM) photograph of the defined channel waveguide before the deposition of the upper cladding layer, while Fig. 6 depicts the atomic force microscopy (AFM) picture of a silicon–nitride rib, with width of 4 μm and a height of 1.8 nm.

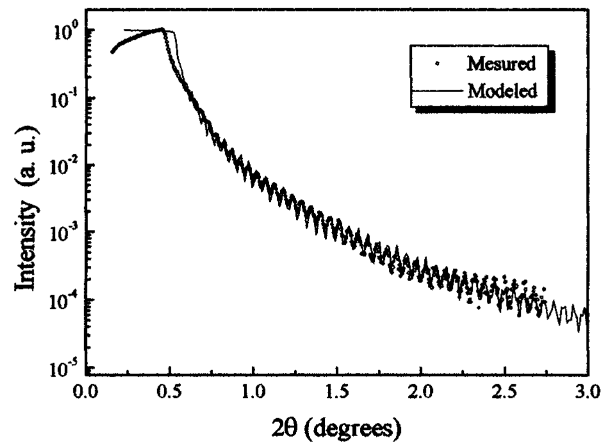

Fig. 3. Measured and modeled reflectivity curves ($GIXR$) of the LPCVD silicon–nitride layer deposited over silicon–oxide buffer layer.

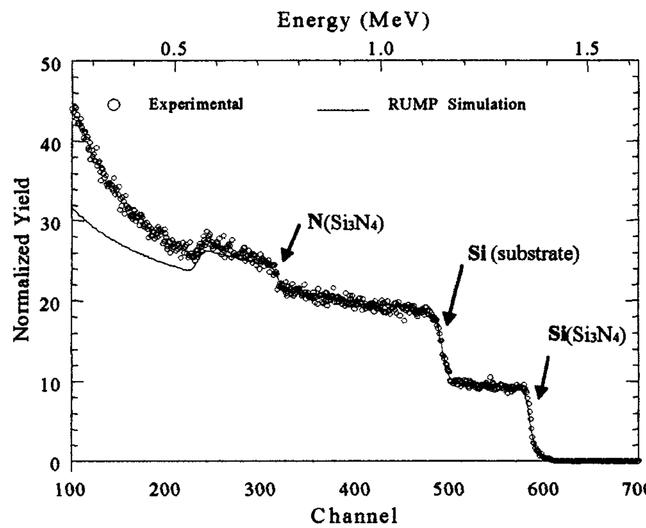

Fig. 4. RBS spectrum of silicon nitride over the silicon substrate.

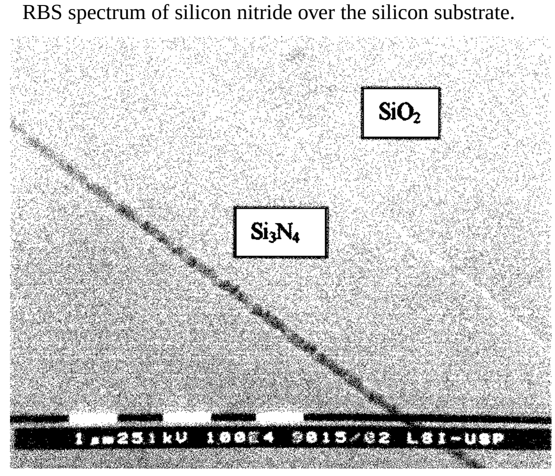

Fig. 5. SEM photograph of a silicon–nitride channel waveguide over the silicon–oxide buffer. This photograph was taken before the deposition of the upper cladding layer.

Refractive index measurements of the fabricated films were carried out by ellipsometry at 632.8 nm. The LPCVD Si_3N_4 LPCVD, thermal SiO_2, and PECVD SiO_2 films showed refractive index of 2.04, 1.46, and 1.44, respectively.

Modal characteristics of the fabricated waveguides were initially evaluated by a numerical extension of the effective index

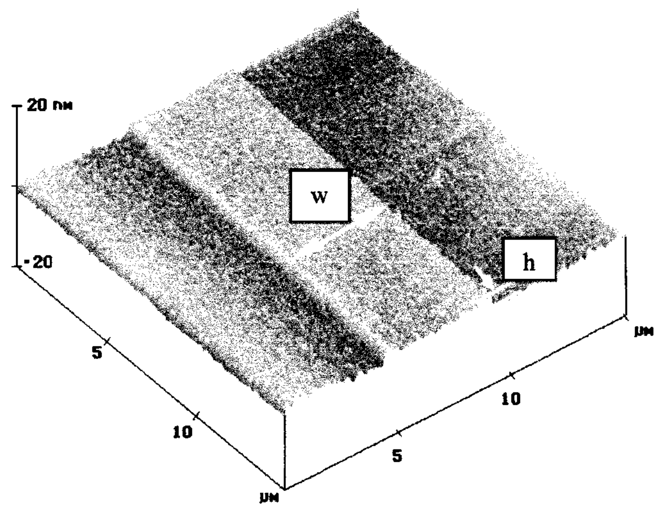

Fig. 6. AFM picture of a silicon–nitride rib waveguide over the silicon–oxide buffer. In this picture, the rib width and height are 4 μm and 1.8 nm, respectively. The AFM procedure was carried out before the deposition of the upper cladding layer.

method [7] and later verified by the projection of the near field of the guided modes at the end of the waveguide. Despite the 0.14-μm core thickness, the high-index contrast of the micrometer-wide channel waveguide produces a multimode structure in the lateral direction. On the other hand, careful control of the etching depth defining the rib height induces a much smaller effective index contrast and allows the fabrication of single-mode rib waveguides.

Optical-loss measurements were carried out by butt coupling the light from an He–Ne laser into the Si_3N_4 films. Assuming that the intensity of scattered light reaching the top surface of the waveguide is directly proportional to the guided optical power [10], a surface scanning was performed along the optical channel by using a microscope objective (40X) coupled to a p-i-n photodetector. A photograph of the experimental arrangement is shown in Fig. 7. Although the use of the 632.8-nm wavelength was dictated mainly by characterization purposes, it is important to note that some applications, such as holographic memories for optical storage, justify the use of wavelengths in the visible range.

An important loss mechanism in integrated optical waveguides is the scattering loss produced at the device interfaces. In planar waveguides, these loss contributions come exclusively from the imperfections introduced during the fabrication process, and are normally small. Channel waveguides, on the other hand, also exhibit a significant amount of loss on the sidewalls of the guide due to the etching process. Depending on the wall roughness, the losses can be prohibitively large. Typical values for the roughness of the walls may range from 30 to 50 nm. In this study, the scattering loss was calculated as follows [11]:

$$\alpha = 4(\beta_z \sigma)^2 \frac{\frac{\cos^3(\theta)}{\sin(\theta)}}{W + \frac{2}{p}} \tag{1}$$

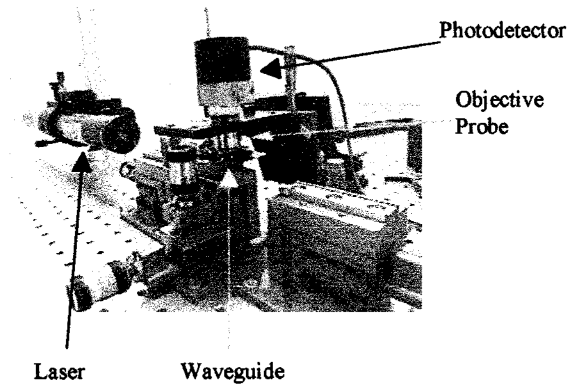

Fig. 7. Experimental arrangement.

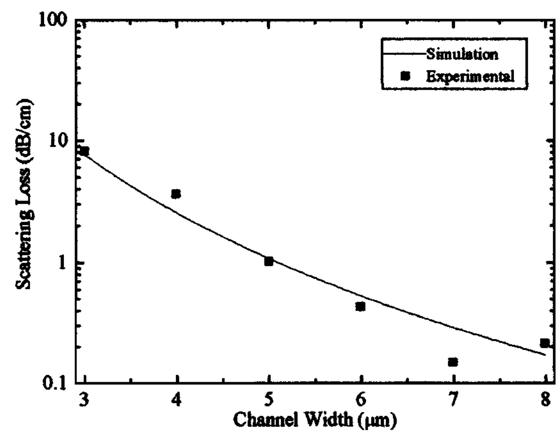

Fig. 8. Scattering loss as a function of the channel width.

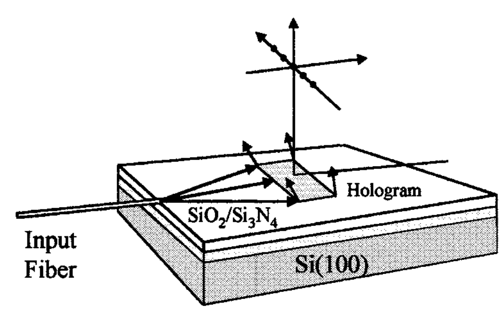

Fig. 9. Schematic outcoupling waveguide hologram.

where β_z is the longitudinal propagation constant, σ is the wall roughness, W is the channel width, p is the decay constant in the cladding, and θ is the propagation angle of the guided light.

A comparison between the experimental results obtained by using the procedure described in the previous section and the theoretical values predicted by the above expression is given in Fig. 8. The close match observed strongly indicates that the optical power loss in the waveguide is fundamentally caused by surface roughness. Thus, the power leakage to the substrate seems to have been effectively suppressed, as desired. Also, the best fitting for the experimental results was obtained for a roughness σ of 35 nm, in the range of the values previously reported in the literature [11]. Finally, it is worth mentioning that, as the channel width increases, the experimental value for the optical loss should reach a plateau dominated by the intrinsic material absorption. Fig. 8 suggests that, in our case, this plateau is around 0.1 dB/cm, the predicted sensitivity of our characterization setup.

Regarding the rib waveguides, our experimental results are not yet conclusive. The very good quality of the lateral etching as well as the reduced sidewall scattering yielded by the field confinement below the rib produced losses that seem to be below the present measurement capability of our experimental arrangement.

IV. Conclusions and Future Outlook

In this paper, silicon-based optical waveguides have been revisited. Power leakage to the substrate has been effectively suppressed by careful design and fabrication procedure. Optical losses have been essentially determined by scattering caused by waveguide wall roughness and the measurement limit of 0.1 dB/cm allowed by our experimental setup has been achieved. Optical interconnects applications involving the use of vertical cavity surface-emitting lasers (VCSELs) will suffer from slightly higher scattering losses due to the smaller modal confinement at the longer 850-nm wavelength, inducing a larger interaction of the optical field with the waveguide sidewalls.

The fabricated waveguides are now being investigated for use on a free-space optical interconnection arrangement, the so-called “off-plane waveguide hologram” [12], illustrated in Fig. 9, where the hologram is etched on the waveguide surface for the outcoupling of the guided wave. Research is under way to assess the overall performance of the hologram-waveguide combination. In contrast to the usual phase-only approach, the wavefronts leaving each hologram pixel are both phase and amplitude modulated.

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Douglas Anderson Pereira Bulla was born in Santa Fé do Sul, Brazil, in 1958. He received the B.Sc. degree in physics from the Pontifical Catholic University of São Paulo, São Paulo SP, Brazil, in 1984, and the M.Sc. degree in physics and the D.Sc. degree in electrical engineering from the University of São Paulo, São Paulo SP, Brazil, in 1988 and 1999, respectively.

He is currently a Post-Doctoral Fellow involved with the design and fabrication of silica-based integrated optics and diffractive optical devices at the University of São Paulo, São Paulo SP, Brazil.

Ben-Hur Viana Borges was born in Governador Valadares, Brazil, in 1963. He received the B.Sc. degree in electrical engineering from the Universidade do Vale do Rio Doce, Governador Valadares, Brazil, in 1987, the M.Sc. degree in electrical engineering from the University of São Paulo, São Carlos SP, Brazil, in 1992, and the Ph.D. degree from Drexel University, Philadelphia, PA, in 1997.

He is currently with the University of São Paulo, São Carlos SP, Brazil. His interests include modeling of linear and nonlinear optical waveguides, grating assisted devices, electrooptic modulators, fiber-optic sensors, and integrated optic sensors.

Murilo Araujo Romero was born in Rio de Janeiro, Brazil, in 1965. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Pontifical Catholic University of Rio de Janeiro, Rio de Janeiro, Brazil, in 1988 and 1991, respectively, and the Ph.D. degree from Drexel University, Philadelphia, PA, in 1995.

He is currently an Associate Professor of electrical engineering, at the University of São Paulo, São Carlos SP, Brazil. His current research interests are focused on optical communications, as well as on the modeling and simulation of opto-electronic semiconductor devices and circuits

Nilton Itiro Morimoto was born in São Paulo, Brazil, in 1962. He received the B.Sc. degree in physics, and the M.Sc. and D.Sc. degrees in electrical engineering from the University of São Paulo, São Paulo SP, Brazil, in 1984, 1987, and 1995, respectively.

His research interests focus on material processing for microelectronic and integrated-optics devices.

Luiz Gonçalves Neto was born in São Paulo, Brazil, in 1962. He received the B.Sc. degree in electrical engineering from the University of São Paulo, São Carlos SP, Brazil, in 1985, the M.Sc. degree in physics from the Instituto de Física de São Carlos, University of São Paulo, São Carlos SP, Brazil, in 1990, and the Ph.D. degree in physics from the Centre d’Optique, Photonique et Laser, Laval University, Quebec, QC, Canada, in 1996.

In 1997, he rejoined the University of São Paulo, as an Assistant Professor, where he conducts research on diffractive optics, computer-generated holograms, spatial light modulators, optical signal processing, pattern recognition, optical interconnects, and optical image encryption.

Dr. Neto is a member of the Optical Society of America (OSA) and The International Society for Optical Engineers (SPIE). He was the recipient of the DOMO 2000 Diffractive Beauty Contest—Artistic Division, sponsored by the OSA.